8086/8088 Hardware Specifications
Introduction

- In this chapter, the pin functions of both the 8086 and 8088 microprocessors are detailed and information is provided on the following hardware topics: clock generation, bus buffering, bus latching, timing, wait states, and minimum mode operation versus maximum mode operation.

- These simple microprocessors are explained as an introduction to the Intel microprocessor family.
In this section, we explain the function and the **multiple functions** of each of the microprocessor’s pins.

In addition, we discuss the **DC characteristics** to provide a basis for understanding the later sections on **buffering** and **latching**.
The Pin-Out

- Figure 1 illustrates pin-outs of 8086 & 8088.
  - both are packaged in 40-pin **dual in-line** packages (DIPs)
- 8086 is a **16-bit** microprocessor with a 16-bit data bus; 8088 has an **8-bit** data bus.
  - 8086 has pin connections $AD_0$–$AD_{15}$
  - 8088 has pin connections $AD_0$–$AD_7$
- Data bus width is the only major difference.
  - thus 8086 transfers 16-bit data more efficiently
Figure 1  (a) The pin-out of the 8086 in **maximum mode**; (b) the pin-out of the 8086 in **minimum mode**.
Power Supply Requirements

- Both microprocessors require +5.0 V with a supply voltage tolerance of ±10 percent.
  - 8086 uses a maximum supply current of 360 mA
  - 8088 draws a maximum of 340 mA
- Both microprocessors operate in ambient temperatures of between 32° F and 180° F.
- 80C88 and 80C86 are CMOS versions that require only 10 mA of power supply current.
  - and function in temperature extremes of −40° F through +225° F
DC Characteristics

• It is impossible to connect anything to a microprocessor without knowing input current requirement for an input pin.
  – and the output current drive capability for an output pin

• This knowledge allows hardware designers to select proper interface components for use with the microprocessor
  – without the fear of damaging anything
Input Characteristics

- Input characteristics of these microprocessors are compatible with all the standard logic components available today.

- Table 1 depicts input voltage levels and the input current requirements for any input pin on either microprocessor.

- The input current levels are very small because the inputs are the gate connections of MOSFETs and represent only leakage currents.
Output Characteristics

• Table 2 illustrates output characteristics of all the output pins of these microprocessors.
• The logic 1 voltage level of the 8086/8088 is compatible with most standard logic families.
  – logic 0 level is not
• Standard logic circuits have a maximum logic 0 voltage of 0.4 V; 8086/8088 has a maximum of 0.45 V.
  – a difference of 0.05 V
• This difference reduces the noise immunity from 400 mV (0.8 V – 0.45 V) to 350 mV.
  – noise immunity is the difference between logic 0 output voltage and logic 0 input voltage levels

• Reduction in noise immunity may result in problems with long wire connections or too many loads.

• No more than 10 loads of any type should be connected to an output pin without buffering
  – if this factor is exceeded, noise will begin to take its toll in timing problems
Pin Connections \( \text{AD}_7 - \text{AD}_0 \)

- 8088 **address/data bus** lines are multiplexed
  - and contain the rightmost 8 bits of the memory address or I/O port number whenever ALE is active (logic 1)
  - or data whenever ALE is inactive (logic 0)
- These pins are at their high-impedance state during a hold acknowledge.
Pin Connections $A_{15} - A_8$

- 8088 **address bus** provides the upper-half memory address bits that are present throughout a bus cycle.
- These address connections go to their **high-impedance state** during a hold acknowledge.
Pin Connections AD\textsubscript{15} - AD\textsubscript{8}

- 8086 \textcolor{red}{address/data bus} lines compose upper multiplexed address/data bus on the 8086.
- These lines contain address bits A\textsubscript{15}–A\textsubscript{8} whenever \textcolor{red}{ALE} is a logic 1, and data bus connections D\textsubscript{15}–D\textsubscript{8} when \textcolor{red}{ALE} is a logic 0.
- These pins enter a \textcolor{red}{high-impedance state} when a hold acknowledge occurs.
Pin Connections $A_{19}/S_6 - A_{16}/S_3$

- **Address/status bus** bits are multiplexed to provide address signals $A_{19} - A_{16}$ and status bits $S_6 - S_3$.
  - high-impedance state during hold acknowledge
  - status bit $S_6$ is always logic 0,
  - bit $S_5$ indicates the condition of the IF flag bit

- $S_4$ and $S_3$ show which segment is accessed during the current bus cycle.
  - these **status bits** can address four separate 1M byte memory banks by decoding as $A_{21}$ and $A_{20}$
Pin Connections \( \overline{RD} \)

- When \textbf{read signal} is logic 0, the data bus is receptive to data from memory or I/O devices
  - pin floats high-impedance state during a hold acknowledge

Ready

- \textbf{ Inserts wait states into the timing.}
  - if placed at a logic 0, the microprocessor enters into wait states and remains idle
  - if logic 1, no effect on the operation
Pin Connections INTR

- **Interrupt request** is used to request a hardware interrupt.
  - If INTR is held high when IF = 1, 8086/8088 enters an interrupt acknowledge cycle after the current instruction has completed execution.

NMI

- The **non-maskable interrupt** input is similar to INTR.
  - does not check IF flag bit for logic 1
  - if activated, uses interrupt vector 2
Pin Connections TEST

- The **Test** pin is an input that is tested by the WAIT instruction.
- If **TEST** is a logic 0, the WAIT instruction functions as an NOP.
- If **TEST** is a logic 1, the WAIT instruction waits for **TEST** to become a logic 0.
- The **TEST** pin is most often connected to the 8087 numeric coprocessor.
Pin Connections RESET

- Causes the microprocessor to reset itself if held high a minimum of four clocking periods.
  - when 8086/8088 is reset, it executes instructions at memory location FFFFOH
  - also disables future interrupts by clearing IF flag

CLK

- The clock pin provides the basic timing signal.
  - must have a duty cycle of 33 % (high for one third of clocking period, low for two thirds) to provide proper internal timing
Pin Connections VCC

• This **power supply** input provides a +5.0 V, ±10 % signal to the microprocessor.

GND

• The **ground** connection is the return for the power supply.
  – 8086/8088 microprocessors have two pins labeled GND—both must be connected to ground for proper operation
Pin Connections MN/MX

- **Minimum/maximum** mode pin selects either minimum or maximum mode operation.
  - if minimum mode selected, the MN/MX pin must be connected directly to +5.0 V

BHE $S_7$

- The **bus high enable** pin is used in 8086 to enable the most-significant data bus bits ($D_{15}–D_8$) during a read or a write operation.
- The state of $S_7$ is always a logic 1.
Minimum Mode Pins

- Minimum mode operation is obtained by connecting the MN/MX pin directly to +5.0 V.
  - do not connect to +5.0 V through a pull-up register; it will not function correctly

IO/M or M/IO

- The IO/M (8088) or M/IO (8086) pin selects memory or I/O.
  - indicates the address bus contains either a memory address or an I/O port address.
  - high-impedance state during hold acknowledge
Minimum Mode Pins  **WR**

- **Write line** indicates 8086/8088 is outputting data to a memory or I/O device.
  - during the time WR is a logic 0, the data bus contains valid data for memory or I/O
  - high-impedance during a hold acknowledge

**INTA**

- The **interrupt acknowledge** signal is a response to the **INTR** input pin.
  - normally used to gate the interrupt vector number onto the data bus in response to an interrupt
Minimum Mode Pins ALE

- **Address latch enable** shows the 8086/8088 address/data bus contains an address.
  - can be a memory address or an I/O port number
  - ALE signal doesn’t float during hold acknowledge

DT/\bar{R}

- The **data transmit/receive** signal shows that the microprocessor data bus is transmitting \( DT/\bar{R} = 1 \) or receiving \( DT/\bar{R} = 0 \) data.
  - used to enable external data bus buffers
Minimum Mode Pins DEN

• **Data bus enable** activates external data bus buffers.

HOLD

• **Hold input** requests a direct memory access (DMA).
  – if HOLD signal is a logic 1, the microprocessor stops executing software and places address, data, and control bus at high-impedance
  – if a logic 0, software executes normally
Minimum Mode Pins HLDA

- **Hold acknowledge** indicates the 8086/8088 has entered the hold state.

**SS0**

- The SS0 status line is equivalent to the $S_0$ pin in maximum mode operation.
- **Signal** is combined with $IO\overline{M}$ and $DT\overline{R}$ to decode the function of the current bus cycle.
**Maximum Mode Pins**

- In order to achieve maximum mode for use with external coprocessors, connect the MN/MX pin to ground.

**S2, S1, and S0**

- **Status bits** indicate function of the current bus cycle.
  - normally decoded by the 8288 bus controller
Maximum Mode Pins RQ/GT1

- The **request/grant** pins request direct memory accesses (DMA) during maximum mode operation.
  - bidirectional; used to request and grant a DMA operation

LOCK

- The **lock** output is used to lock peripherals off the system. This pin is activated by using the LOCK: prefix on any instruction.
Maximum Mode Pins $QS_1$ and $QS_0$

- The **queue status** bits show the status of the internal instruction queue.
  - provided for access by the 8087 coprocessor
CLOCK GENERATOR (8284A)

• This section describes the 8484A clock generator and the RESET signal.
  – also introduces the READY signal for 8086/8088

• With no clock generator, many circuits would be required to generate the clock (CLK).

• 8284A provides the following basic functions:
  – clock generation; RESET & READY synch;
  – TTL-level peripheral clock signal

• Figure 2 shows pin-outs of the 8284A
Figure 2  The pin-out of the 8284A clock generator.
8284A Pin Functions

• 8284A is an 18-pin integrated circuit designed specifically for use 8086/8086.

AEN1 and AEN2

• The **address enable** pins are provided to qualify bus ready signals, RDY1 and RDY2.
  – used to cause wait states
• **Wait states** are generated by the READY pin of 8086/8088 controlled by these two inputs.
**Pin Functions** \(RDY_1\) and \(RDY_2\)

- The **bus ready** inputs are provided, in conjunction with the \(AEN1\) & \(AEN2\) pins, to cause wait states in 8086/8088.

**ASYNC**

- The **ready synchronization** selection input selects either one or two stages of synchronization for the \(RDY_1\) and \(RDY_2\) inputs.
**Pin Functions READY**

- **8284 Ready** is an output pin that connects to the 8086/8088 READY input.
  - synchronized with the RDY₁ and RDY₂ inputs

**X₁ and X₂**

- The **crystal oscillator** pins connect to an external crystal used as the timing source for the clock generator and all its functions
Pin Functions F/Ć

- The **frequency/crystal** select input chooses the clocking source for the 8284A.
  - if held high, an **external clock** is provided to the EFI input pin
  - if held low, the **internal crystal oscillator** provides the timing signal
- The external frequency input is used when the **F/Ć** pin is pulled high.
- EFI supplies timing when the **F/Ć** pin is high.
Pin Functions CLK

- The **clock output** pin provides the CLK input signal to 8086/8088 and other components.
  - output signal is one third of the crystal or EFI input frequency
  - 33% duty cycle required by the 8086/8088

PCLK

- The **peripheral clock** signal is one sixth the crystal or EFI input frequency.
  - PCLK output provides a clock signal to the peripheral equipment in the system
Pin Functions OSC

- **Oscillator output** is a TTL-level signal at the same frequency as crystal or EFI input.
  - OSC output provides EFI input to other 8284A clock generators in multiple-processor systems

RES

- **Reset input** is an active-low input to 8284A.
  - often connected to an RC network that provides power-on resetting
Pin Functions RESET

- **Reset output** is connected to the 8086/8088 RESET input pin.

CSYNCH

- The **clock synchronization** pin is used when the EFI input provides synchronization in systems with multiple processors.
  - if internal crystal oscillator is used, this pin must be grounded
Pin Functions GND

- The **ground pin** connects to ground.

VCC

- This **power supply** pin connects to +5.0 V with a tolerance of ±10%.
Operation of the 8284A

- The 8284A is a relatively easy component to understand.
- Figure 3 illustrates the internal timing diagram of the 8284A clock generator.
- The top half of the logic diagram represents the clock and synchronization section of the 8284A clock generator.
Figure 3 The internal block diagram of the 8284A clock generator.
Operation of the Clock Section

• Crystal oscillator has two inputs: \( X_1 \) and \( X_2 \).
  – if a crystal is attached to \( X_1 \) and \( X_2 \), the oscillator generates a square-wave signal at the same frequency as the crystal

• The square-wave is fed to an AND gate & an inverting buffer to provide an OSC output.

• The OSC signal is sometimes used as an EFI input to other 8284A circuits in a system.

• Figure 4 shows how an 8284A is connected to the 8086/8088.
Figure 4  The clock generator (8284A) and the 8086 and 8088 microprocessors illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor.
Operation of the Reset Section

• The reset section of 8284A consists of a Schmitt trigger buffer and a D-type flip-flop.
  – the D-type flip-flop ensures timing requirements of 8086/8088 RESET input are met
• This circuit applies the RESET signal on the negative edge (1-to-0 transition) of each clock.
• 8086/8088 microprocessors sample RESET at the positive edge (0-to-1 transition) clocks.
  – thus, this circuit meets 8086/8088 timing requirements
BUS TIMING

• It is essential to understand system bus timing before choosing memory or I/O devices for interfacing to 8086 or 8088 microprocessors.
• This section provides insight into operation of the bus signals and the basic read/write timing of the 8086/8088.
Basic Bus Operation

• The three buses of 8086/8088 function the same way as any other microprocessor.

• If data are written to memory the processor:
  – outputs the memory address on the address bus
  – outputs the data to be written on the data bus
  – issues a write (WR) to memory
  – and IO/\bar{M}= 0 for 8088 and IO/\bar{M} = 1 for 8086

• See simplified timing for write in Fig 5.
Figure 5  Simplified 8086/8088 write bus cycle.
• If data are read from the memory the microprocessor:
  – outputs the memory address on the address bus
  – issues a read memory signal (RD)
  – and accepts the data via the data bus
• See simplified timing for read in Fig 6.
Figure 6  Simplified 8086/8088 read bus cycle.
Timing in General

• 8086/8088 use memory and I/O in periods called bus cycles.
• Each cycle equals four system-clocking periods (T states).
  – newer microprocessors divide the bus cycle into as few as two clocking periods
• If the clock is operated at 5 MHz, one 8086/8088 bus cycle is complete in 800 ns.
  – basic operating frequency for these processors
• During the **first** clocking period in a bus cycle, called **T1**, many things happen:
  – the **address** of the memory or I/O location is sent out via the address bus and the address/data bus connections.

• **During T1**, **control signals** are also output.
  – indicating whether the address bus contains a memory address or an I/O device (port) number

• **During T2**, the processors issue the **RD** or **WR** signal, **DEN**, and in the case of a write, the data to be written appear on the data bus.
• These events cause the memory or I/O device to begin to perform a read or a write.

• **READY** is sampled at the end of $T_2$.
  – if low at this time, $T_3$ becomes a wait state ($T_w$)
  – this clocking period is provided to allow the memory time to access data

• If a read bus cycle, the data bus is sampled at the end of $T_3$.

• Illustrated in Figure 7.
Figure 7 Minimum mode 8088 bus timing for a read operation.

- In $T_4$, all bus signals are deactivated in preparation for the next bus cycle.
- Data bus connections are sampled for data read from memory or I/O.
Read Timing

- Figure 7 also depicts 8088 read timing.
  - 8086 has 16 rather than eight data bus bits
- Important item in the read timing diagram is time allowed for memory & I/O to read data.
- Memory is chosen by its access time.
  - the fixed amount of time the microprocessor allows it to access data for the read operation
- It is extremely important that memory chosen complies with the limitations of the system.
• The microprocessor timing diagram does not provide a listing for memory access time.
  – necessary to combine several times to arrive at the access time

• Memory **access time** starts when the address appears on the memory address bus and continues until the microprocessor **samples** the memory **data** at $T_3$.
  – about three $T$ states elapse between these times

• The address does not appear until $T_{CLAV}$ time (110 ns if a 5 MHz clock) after the start of $T_1$. 
• $T_{\text{CLAV}}$ time must be subtracted from the three clocking states (600 ns) separating the appearance of the address ($T_1$) and the sampling of the data ($T_3$).

• The **data setup time** ($T_{\text{DVCL}}$), which occurs before $T_3$ must also be subtracted.

• Memory access time is thus three clocking states minus the sum of $T_{\text{CLAV}}$ and $T_{\text{DVCL}}$.

• Because $T_{\text{DVCL}}$ is 30 ns with a 5 MHz clock, the allowed memory access time is only 460 ns (**access time** $= 600 \text{ ns} - 110 \text{ ns} - 30 \text{ ns}$).
• To find memory access time in this diagram:
  – locate the point in \( T_3 \) when data are sampled
  – you will notice a line that extends from the end of \( T_3 \) down to the data bus
  – at the end of \( T_3 \), the microprocessor samples the data bus.
• Memory devices chosen for connection to the 8086/8088 operating at 5 MHz must be able to access data in less than 460 ns.
  – because of the **time delay** introduced by the address decoders and buffers in the system
  – a 30- or 40-ns **margin** should exist for the operation of these circuits
• The memory speed should be **no slower than** about 420 ns to operate correctly with the 8086/8088 microprocessors.
Strobe Width

• The other timing factor to affect memory operation is the width of the $\overline{RD}$ strobe.
• On the timing diagram, the read strobe is given as $T_{RLRHZ}$.
• The time for this strobe at a 5 MHz clock rate is 325 ns.
• This is wide enough for almost all memory devices manufactured with an access time of 400 ns or less.
Write Timing

• Figure 9 illustrates 8088 write-timing.
  – 8086 is nearly identical

• The RD strobe is replaced by the WR strobe,
  – the data bus contains information for the memory rather than information from the memory,
  – DT/R remains a logic 1 instead of a logic 0 throughout the bus cycle

• When interfacing some devices, timing may be critical between when WR becomes logic 1 and the data are removed from the data bus.
Figure 9 Minimum mode 8088 write bus timing.

**NOTES:**

1. All signals switch between $V_{OH}$ and $V_{OL}$ unless otherwise specified.
2. RDY is sampled near the end of $T_2$, $T_3$, $T_W$ to determine if $T_W$ machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 8088 local ADDR/DATA bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at 8284 are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.
• Memory data are written at the trailing edge of the WR strobe.
• On the diagram, this critical period is $T_{WHDX}$ or 88 ns when 8088 on a 5 MHz clock.
• Hold time is often less than this.
  – in fact often 0 ns for memory devices
• The width of the WR strobe is $T_{WLWH}$ or 340 ns with a 5 MHz clock.
• This rate is compatible with most memory devices with access time of 400 ns or less.
READY AND THE WAIT STATE

- The READY input causes wait states for slower memory and I/O components.
  - A wait state ($T_w$) is an extra clocking period between $T_2$ and $T_3$ to lengthen bus cycle.
  - On one wait state, memory access time of 460 ns, is lengthened by one clocking period (200 ns) to 660 ns, based on a 5 MHz clock.
- This section covers READY synchronization circuitry inside the 8284A clock generator.
The READY Input

• The READY input is sampled at the end of $T_2$ and again, if applicable, in the middle of $T_w$.
• The READY input to 8086/8088 has stringent timing requirements.
• Fig 10 shows READY causing one wait state ($T_w$), with the required setup and hold times from the system clock.
• When the 8284A is used for READY, the RDY (ready input to 8284A) input occurs at the end of each T state.
Figure 10  8086/8088 READY input timing.

- If READY is logic 0 at the end of $T_2$, $T_3$ is delayed and $T_w$ inserted between $T_2$ and $T_3$.
- READY is next sampled at the middle of $T_w$ to determine if the next state is $T_w$ or $T_3$. 
RDY and the 8284A

- RDY is the synchronized ready input to the 8284A clock generator.
- Internal 8284A circuitry guarantees the accuracy of the READY synchronization.

Figure 11 8284A RDY input timing.
• Fig 12 depicts internal structure of 8284A.
  – the bottom half is the READY synch circuitry
• Fig 13 shows a circuit to introduce almost any number of wait states to 8086/8088.
• An 8-bit serial shift register (74LS164) shifts a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A.
• With appropriate strapping, this circuit can provide various numbers of wait states.
Figure 12 The internal block diagram of the 8284A clock generator. (Courtesy of Intel Corporation.)
Figure 13  A circuit that will cause between 0 and 7 wait states.
• Note in Fig 13 that this circuit is enabled only for devices that need insertion of waits.
  – if the selection signal is a logic 0, the device is selected and this circuit generates a wait state
• Figure 14 shows timing of this shift register wait state generator when wired to insert one wait state.
• The timing diagram also illustrates the internal contents of the shift register’s flip-flops
  – to present a more detailed view of its operation
• In this example, one wait state is generated.
Figure 14 Wait state generation timing of the circuit of Figure 13.
MINIMUM VS MAXIMUM MODE

• **Minimum mode** is obtained by connecting the mode selection **MN/MX** pin to **+5.0 V**,  
  – maximum mode selected by grounding the pin

• The mode of operation provided by minimum mode is similar to that of the **8085A**  
  – the most recent Intel 8-bit microprocessor

• **Maximum mode** is designed to be used whenever a **coprocessor** exists in a system.  
  – maximum mode was dropped with **80286**
Minimum Mode Operation

• Least expensive way to operate 8086/8088.
  – because all control signals for the memory & I/O are generated by the microprocessor

• Control signals are identical to Intel 8085A.

• The **minimum mode** allows 8085A 8-bit peripherals to be used with the 8086/8088 without any special considerations.
Figure 15  Minimum mode 8088 system.
Maximum Mode Operation

• Differs from minimum mode in that some control signals must be externally generated.
  – requires addition of the 8288 bus controller

• There are not enough pins on the 8086/8088 for bus control during maximum mode
  – new pins and features replaced some of them

• Maximum mode used only when the system contains external coprocessors such as 8087.
Figure 16 Maximum mode 8088 system.
The 8288 Bus Controller

- Provides the signals eliminated from the 8086/8088 by the maximum mode operation.

Figure 17 The 8288 bus controller; (a) block diagram and (b) pin-out.
8288 Bus Controller *Pin Functions*

*S₂, S₁, and S₀*

- **Status inputs** are connected to the status output pins on 8086/8088.
  - three signals decoded to generate timing signals

**CLK**

- **The clock** input provides internal timing.
  - must be connected to the CLK output pin of the 8284A clock generator
8288 Bus Controller *Pin Functions*

**ALE**

- The **address latch enable** output is used to demultiplex the address/data bus.

**DEN**

- The **data bus enable** pin controls the bidirectional data bus buffers in the system.

**DT/\bar{R}**

- **Data transmit/receive** signal output to control direction of the bidirectional data bus buffers.
8288 Bus Controller *Pin Functions*

**AEN**
- The **address enable** input causes the 8288 to enable the memory control signals.

**CEN**
- The **control enable** input enables the command output pins on the 8288.

**IOB**
- The **I/O bus mode** input selects either I/O bus mode or system bus mode operation.
8288 Bus Controller *Pin Functions*

**AIOWC**

- **Advanced I/O write** is a command output to an advanced I/O write control signal.

**IORC**

- The **I/O read command** output provides I/O with its read control signal.

**IOWC**

- The **I/O write command** output provides I/O with its main write signal.
8288 Pin Functions

AMWT
- **Advanced memory write** control pin provides memory with an early/advanced write signal.

MWTC
- The **memory write** control pin provides memory with its normal write control signal.

MRDC
- The **memory read** control pin provides memory with a read control signal.
8288 Bus Controller *Pin Functions*

**INTA**

- The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.

**MCE/PDEN**

- The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.
Pin Functions

The following list provides a description of each pin of the 8288 bus controller.

$S_2$, $S_1$, and $S_0$ **Status inputs** are connected to the status output pins on the 8086/8088 microprocessor. These three signals are decoded to generate the timing signals for the system.

**CLK**
The clock input provides internal timing and must be connected to the CLK output pin of the 8284A clock generator.

**ALE**
The **address latch enable** output is used to demultiplex the address/data bus.

**DEN**
The **data bus enable** pin controls the bidirectional data bus buffers in the system. Note that this is an active high output pin that is the opposite polarity from the **DEN** signal found on the microprocessor when operated in the minimum mode.

**DT/R**
The **data transmit/receive** signal is output by the 8288 to control the direction of the bidirectional data bus buffers.

**AEN**
The **address enable** input causes the 8288 to enable the memory control signals.

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The **control enable** input enables the command output pins on the 8288.

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The **I/O bus mode** input selects either the I/O bus mode or system bus mode operation.

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The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.

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The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.
THE END